

Technology Overview: VITA 46 (VPX)

INTRODUCTION

This Mercury Technology Overview is one in a series designed to provide a deeper look at the array of Mercury technologies available to designers of high-performance signal processing systems.

In this overview, we look at VITA 46 (VPX), a new computing standard that combines the latest in connector and packaging technology with the latest in serial fabric and bus technology. We discuss the motivation behind creating a new standard, the primary issues its architects were trying to solve, and some points in the architecture that may help decisions on implementing systems using the standard. To get the most from this overview, you should already be familiar with these resources:

- Mercury Technology Brief: Evolution of Computing Standards for Signal Processing
- Any of several computing standards based on the popular Eurocard format, such as VME64x or CompactPCI®

This overview does not represent the complete technical detail available in the specifications discussed, but it does draw on information from those specifications. Copies of complete specifications are available for purchase upon release as ANSI standards from VITA, the trade association responsible for their development, at www.vita.com.

CREATING VPX

VMEbus technology continues to be the choice for systems that require high performance, longer life cycles, durability and a highly flexible combination of technology from which systems designers can choose.

VPX strives to introduce a new breakthrough in embedded computing standards, creating an all-new best-practice specification leveraging 25 years of VMEbus technology while incorporating lessons learned and enhancing the platform with needed improvements and new innovations. Its goal is to create an evolutionary path for today's VMEbus users and set the stage for the next 25 years of use. By combining the latest in connector and packaging technology with the latest in bus and serial fabric technology, the architects of VPX have crafted a standard that fills both the needs of mass-market commercial platforms for industrial and medical use, and the requirements of Commercial-off-the-Shelf (COTS) platforms for defense and aerospace.

There are several motivations behind the creation of VPX:

High-density, high-performance computing – Size and weight-constrained applications call for a new standard, with lessons learned from previous efforts. Many mobile applications such as aircraft, ground vehicles, and even human transportable systems are very space-constrained. VPX leverages the existing IEEE 1101 3U or 6U form factor with commonality, enables heterogeneous architectures to help preserve existing investments in technology and systems, and reflects systems thinking in rear-panel

I/O and maintenance strategies. Complex algorithms and multiple high-speed data sources require high performance.

Improved bandwidth – Using a choice of modern serial fabric interconnects, system designers have access to dramatically improved bandwidth at greatly reduced pin counts. Compared to VMEbus bandwidths in the 40-60MB range, VPX systems can achieve over 5 Gigabytes per second (5 GB/s) using today's fabric speeds. One key difference in the architecture of VPX is its ability to support an expansive full-mesh design through an increased number of serial fabric links on the module, dramatically increasing system aggregate bandwidth to over 100 GB/s.

Next-generation interconnects like RapidIO® and 10GbE use the XAUI electrical specification running at 3.125 Gigabits per second (Gb/s). Other serial technologies are in a similar range – for example, PCI Express® at 2.5 Gb/s, and Fibre Channel at 4 Gb/s. The latest generation of IEEE1394 cameras can produce image data at well over 1 GB/s. All of these devices operate above the 1 Gb/s limit of the DIN connectors found in VME64x systems. This limitation of the VME64x architecture pushes VME technology architects to some type of new connector, with the choice now whether to incrementally improve with an enhanced P0 or evolve all the pins to a newer connector set.

More sensor data, larger digital images, larger databases, and all-to-all communications are all factors driving the need for more bandwidth.

Increased power – Designers using today's class of powerful processors are finding the VME64x specification of 35W power inflow limiting. Next-generation processors from companies including Freescale™, Intel®, and IBM®, while offering new heights of compute power via multiple cores, stress or exceed the available VME64x power budget. Microprocessor power budgets are not expected to decrease anytime soon, and multi-core architectures do not eliminate the power concerns. By crafting a new specification with increased power inlet and better cooling capabilities such as conduction and liquid methods, VPX can satisfy very demanding applications while still retaining the ability to be cost-effective at the lower end of the performance curve.

Rugged and maintainable COTS – With accommodations for harsh environments and two-level maintenance designed into the specifications, VPX directly targets COTS applications in defense and aerospace. VPX is complimentary to Ruggedized Enhanced Design Implementation (REDI) defined in VITA 48. REDI standardizes features in the mechanical and thermal domain to build upon IEEE 1101's deployability in harsh environments. REDI provides a configuration level which is mechanically compatible with VPX modules. VPX-REDI modules introduce industry standard enhancements that include full compatibility with two-level maintenance, liquid cooling, wider module and backplane slot pitch and more.

Many other application segments have similar durability and maintenance issues and could take advantage of VPX.

OVERVIEW OF VPX

VPX is based on the VITA 46 family of specifications. Architects created VPX as a series of “dot” specifications; a base specification describes common elements, while extension specifications define the use of specific serial fabrics, mapping of VMEbus signals, mapping of PMC and XMC modules, rear transition modules, keying and other topics as needed. Current VITA 46 specifications include:

- VITA 46.0 VPX
- VITA 46.1 VMEbus Signal Mapping for VITA 46
- VITA 46.3 Serial RapidIO on VITA 46
- VITA 46.5 Hypertransport on VITA 46
- VITA 46.9 XMC and PMC User I/O Mapping for VITA 46
- VITA 46.10 Rear Transition Module for VITA 46

VPX Module

The VPX base specification introduces a new module format based on familiar IEEE 1101 Eurocard mechanicals and using a new set of high-speed differential signaling connectors. The base specification provides a common set of definitions for physical characteristics of modules and backplanes, on which dot specifications for implementation of specific switched serial fabric technology can be overlaid.

A VPX module can be either 3U or 6U in width, both formats being 160mm deep with a 4HP (20.32 mm or 0.8”) pitch between slots.

On the 3U format, three connectors are presented: P0, the utility connector, and P1 and P2, the signaling connectors:

- P0 is a 56-pin connector containing power, ground, geographic addressing, system management, system reset, and reference clock signals, along with non-volatile memory write-prevention and JTAG signals.
- P1 is a 112-pin differential signaling connector where signals for serial fabrics are mapped by VPX dot specifications.
- P2 is a 112-pin user-defined connector which can be configured for either single-ended or differential signaling.

On the 6U format, additional 112-pin connectors P3 through P6 for signaling are presented:

- P3 through P6 can be defined as single-ended or differential. In differential mode, one row of P3 through P5 is reserved for single-ended signals.
- P5 and P6 can also be used for non-compatible formats such as optical or coaxial connections.

Combined alignment/keying structures are also defined for VPX modules. Alignment/keying devices are required by the base specification, with two on a 3U module and three on a 6U module. Since each keying device can be fabricated in one of 5 different configurations, VPX supports 25 unique key setting on a 3U card and 125 unique key setting on a 6U card. Differential signaling is important because it allows faster signal switching with a lower signal swing for a given noise immunity. As the signaling speed increases, the slew rate of the signal becomes a limit so lower signaling voltage is needed. Lower voltages reduce noise margin which differential signaling effectively replaces by increasing the effective swing while, at the same time, improving common mode noise rejection. Differential pairing of the signals also allows better control of the signal impedance.

Table 1. VITA 46 and VME64x Compared

Attribute	VME64x	VPX
Bandwidth	320 MB/s using 2eSST	VME: 320 MB/s using 2eSST Fabric: up to 192 differential pairs for signaling 10 GB/s @ 3.125 Gbps 30 GB/s @ 10 Gbps
Switch Fabric	Requires P0 implementation of VITA 31 or VITA 41 (VXS)	Multiple protocols with multiple topologies; Mesh, Star, Dual-Star, Ring, Daisy Chain
Faceplate User I/O	Yes	Yes
Backplane User I/O	205 pins	48 single-ended pins + 192 differential pairs
User I/O for 3U	None	80 pins on J2
Defined PMC Mapping	Single-ended only	Single-ended and differential options
Existing VME64x compatibility	Yes	Yes, with hybrid backplane
Slot Pitch	0.8”	0.8” 0.85” and 1.0” with REDI
Available Power	5V: 90W 3.3V: 66W	5V: 120W 12V: 383W or 48V: 768W
Cooling	Air, conduction	Air, conduction, liquid w/REDI enhancements

MultiGig RT Connector

With increased interconnect speeds, higher pin density and reasonable insertion forces and environmental characteristics as design goals, Tyco undertook development of a new connector family in 2001. Finally dubbed the MultiGig RT family, this new connector is the solution for VPX.

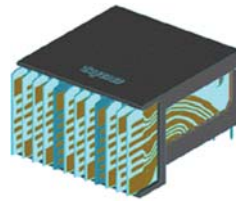


Figure 1. Tyco MultiGig RT Connector

One unique feature of this connector is the “chiclet” design, where contacts and internal routing are formed using miniature printed circuit boards. This design implements several key objectives:

Signal Integrity

Chiclet wafers are available in several formats suited for power, single-ended signaling or differential signaling. Each differential contact pair is currently rated at signal speeds up to 6.25 Gb/s using today’s driver silicon, and it is expected this rating will evolve to 10 Gb/s and over as technology continues to improve.

To affirm integrity, eye pattern testing was performed on a physical backplane with acceptable signal performance found at the rated speeds. Specific test conditions documented by VITA were: 16” FR4 backplane traces, 4” FR4 daughtercard traces, top layer via connection, no counterboring, 27-1 pseudo random bit string. Observed results under these conditions were a 46.8% eye opening.

The MultiGig RT style connector is clearly a significant improvement in signal density and performance over VMEbus options.

Insertion Force

A goal of the VPX design was to create modules that could be inserted and removed using reasonable manual forces generated by the front panel handles. For the VPX module, these are the IEEE 1101.10 handles as found in the VME64x specifications.

Environmental Factors

Durability is a key consideration for system architects looking to use VPX, and the designers of the specification considered this factor strongly in selection of the MultiGig RT connectors.

MultiGig RT connectors are designed for 250 insertion cycles and have been extensively tested in environments according to MIL-STD-1344A, including vibration and shock, thermal shock, humidity, salt fog, dielectric withstanding voltage, low-signal level contact resistance and insulation resistance. These tests were performed by Tyco and augmented by further testing from VPX Working Group members and the U. S. Navy. The conclusions found the MultiGig RT family to be as mechanically robust as the widely accepted, hardy DIN 41612 connectors used in VME64x while able to deliver the advanced electrical performance required for high speed differential signaling.

VPX BACKPLANE

VPX backplanes are defined in terms of compliant dimensions, connectors, power delivery, geographic addressing, required connections (JTAG, system reference clock, non-volatile memory read-only signal, 3.3V auxiliary power intended for system management functions, system reset) and fabric connections. The fabric connection section does not define a topology, but instead specifies signaling parameters intended to support a range of high-speed serial fabrics, discussing signal integrity, materials, routing, length matching, widths, spacing, crosstalk isolation and insertion loss. Common fabric topologies can be supported in VPX: mesh, star, dual-star, ring, and daisy chain as the application requires. Care must be taken in selecting backplane topologies as this may have a significant impact on operation and performance of the system.

VPX does not require that all slots meet the backplane specification, and introduces the notion of a hybrid backplane that has slots for boards compliant with other specifications.

System designers can consider use of boards mapping VMEbus signaling onto VPX connectors (see “Mapping for VMEbus” discussed later in this overview), or hybrid backplanes that implement slots compliant with VME64x, VXS, or other standards.

VPX POWER

VPX introduces new primary power supply inlet voltages, using +5VDC and either +12VDC or +48VDC (but not both as stated by rule). These voltages, along with auxiliary +3.3V and ±12VDC, are presented on P0 with the configuration identified by keying.

VPX allows for significantly higher power inlet than similar Eurocard formats. Using the 48V high voltage rail, up to 768W per slot is allowed. The actual power budget in VPX is likely to be limited by the system’s cooling capability. REDI enhancements including steps such as liquid cooling may be necessary to take full advantage of VPX’s increased power inlet.

VPX COOLING

VPX modules are dimensioned with several cooling strategies in mind, including forced air and conduction cooling. However, specific cooling implementations are not discussed in VPX.

VPX-REDI, also led by the Mercury team, extends the available heights for modules to include the 4HP pitch of 0.8”, and adding 0.85” and 1.00” options. It defines specific implementations of forced air, conduction and liquid cooling. VPX modules are only required to conform to VITA 46. VPX-REDI modules conform to both VITA 46 and VITA 48.

MAPPING FOR SERIAL RAPIDIO

One of the primary goals of VPX was the introduction of high speed serial switched fabrics into the architecture. A “dot” specification, 4x Serial RapidIO Mapping for VPX, extends the architecture and defines use of serial RapidIO as the backplane fabric. Mercury teams led the definition of the VPX mapping for serial RapidIO.

In this mapping, each VPX module supports up to four 4x LP-serial RapidIO links with differential signaling pairs mapped onto P1. These links have been mapped with enough ground pins included to support the high-speed signaling required.

Table 2. VPX Mapping on P1 for Serial RapidIO

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	P1-SE0	GND	PA-TX3-	PA-TX3+	GND	PA-RX3-	PA-RX3+
2	GND	PA-TX2-	PA-TX2+	GND	PA-RX2-	PA-RX2+	GND
3	P1-SE1	GND	PA-TX1-	PA-TX1+	GND	PA-RX1-	PA-RX1+
4	GND	PA-TX0-	PA-TX0+	GND	PA-RX0-	PA-RX0+	GND
5	P1-SE2	GND	PB-TX3-	PA-TX3+	GND	PB-RX3-	PA-RX3+
6	GND	PB-TX1-	PB-TX2+	GND	PB-RX2-	PB-RX2+	GND
7	P1-SE3	GND	PB-TX1-	PB-TX1+	GND	PB-RX1-	PB-RX1+
8	GND	PB-TX0-	PB-TX0+	GND	PB-RX0-	PB-RX0+	GND
9	P1-SE4	GND	PC-TX3-	PC-TX3+	GND	PC-RX3-	PC-RX3+
10	GND	PC-TX2-	PC-TX2+	GND	PC-RX2-	PC-RX2+	GND
11	P1-SE5	GND	PC-TX1-	PC-TX1+	GND	PC-RX1-	PC-RX1+
12	GND	PC-TX0-	PC-TX0+	GND	PC-RX0-	PC-RX0+	GND
13	P1-SE6	GND	PD-TX3-	PD-TX3+	GND	PD-RX3-	PD-RX3+
14	GND	PD-TX2-	PD-TX2+	GND	PD-RX2-	PD-RX2+	GND
15	P1-SE7	GND	PD-TX1-	PD-TX1+	GND	PD-RX1-	PD-RX1+
16	GND	PD-TX0-	PD-TX0+	GND	PD-RX0-	PD-RX0+	GND

VPX MAPPING ON P1 FOR SERIAL RAPIDIO

VPX does not define a backplane topology, but using the mapping of P1 with a total of four 4x serial links, an example topology of a 5-slot full mesh VPX system with a direct connection between each board is illustrated. It is conceivable that a VPX mesh cluster of this order of magnitude could support a TFLOPS or more of processing power. VPX does not define a switch module, although a module with numerous serial links could serve that function in a system. VPX system designers have flexibility in topology for large mesh designs, or designs passing heavy traffic on particular backplane segments, or other topologies such as star, dual-star, daisy chain, or any combination of these.

On a 6U VPX board with all connectors populated, theoretically the P1 definition with four 4x serial RapidIO links could be cloned on P2 through P6 for a total of twenty-four 4x serial RapidIO links. Even considering implementation of parallel bus and I/O mappings on P2, P5 and P6, twelve 4x serial RapidIO

links would be possible. With these types of links available, VPX-compliant systems are theoretically capable of very high aggregate bandwidths, easily exceeding 100 GB/s considering a larger system with multiple modules and simultaneous transactions in progress.

The RapidIO serial physical layer interface offers a XAUI (10G Attachment Unit Interface) compatible electrical interface operating at 1.25, 2.5 or 3.125 Gb/s (with an effective data rate of 2.5 Gb/s after 8b/10b encoding). Because it is XAUI compatible, RapidIO technology is aligned with embedded backplane needs and is able to leverage the volume ecosystem around the XAUI

physical layer. The specification defines one and four lane versions to offer bidirectional bandwidth between 2 Gb/s to 20 Gb/s per link. Four lanes provide a 10 Gb/s port, full duplex. In addition, the serial RapidIO interface can scale incrementally from 1 Gb/s up to 10 Gb/s – offering more flexibility for the designer.

To software, the RapidIO interconnect looks like a traditional microprocessor or peripheral bus, so hardware implementations can hide functions such as discovery and error management from software, unless a software system elects to participate. This is another example of the RapidIO technology's inherent compatibility with legacy system and application software. RapidIO presents a smooth migration path from RACE++® for users of Mercury systems, as applications using the

Parallel Acceleration System/Data Reorganization Interface (PAS™/DRI) library can be recompiled with minimal software changes.

VPX concentrates on the definition of inter-board connections, but one advantage of serial RapidIO is as an intra-board connection. Many of today's advanced processors, such as the Freescale™ MPC8641 dual core PowerPC processor or the Texas Instruments TMS320C6455 DSP offer on-chip serial RapidIO ports with direct connection into the processor. By extending the connections from processors throughout the system via the inter-board backplane and switch card connections, systems can scale their processing power very effectively.

Mercury is a leader in RapidIO, which presents a natural migration path for RACEway users. For a complete discussion of RapidIO technology, visit www.rapidio.org and look in the Education section for the Technology Overview and Applications presentation along with other information.

MAPPING FOR VMEBUS

Even with high-speed serial links available within a system for data transactions, designers often like the option to have a separate path for relatively low-rate control transactions. VMEbus serves this purpose very well, integrating legacy I/O and providing deterministic control operations.

To help fill this need, leverage existing technology and allow designs to evolve, VPX architects created a dot specification that maps VMEbus signals onto VPX modules. This specification maps VMEbus onto P2 of a 3U VPX module, and primarily P2 with some signals on P3, P4 and P5 of a 6U VPX module. This mapping allows VMEbus electrical designs to move into a new, modern layout and leverage the proven VME64x and VME2eSST technology as a parallel bus. Mercury teams led the definition of this mapping specification.

In the VPX mapping for VMEbus, P2 is defined as a single-ended signaling connector. Since P2 has a total of 112 pins, it carries the VME A24:D16 (24-bit address, 16-bit data) signal set, but additional pins are needed to carry the complete VME A32:D32 signal set. These A32:D32 signals are spread over connectors P3, P4 and P5, using the 'G' row of each which was reserved as eight single-ended pins in the base specification. This mapping leaves the differential pairs defined on rows A-F of P3, P4 and P5 in the base specification unaffected. Also unaffected are the entire definitions for P0, P1 and P6 from the base specification.

In this way, the VPX mapping for VMEbus is not only compatible with the VPX base specification but other dot specifications such as the VPX mapping for Serial RapidIO as well.

A major advantage of being able to map VMEbus to VPX is to allow the use of existing hardware and protocols for legacy equipment that does not have the need for VPX. Years of development and system cost can be preserved by bridging to existing VME systems.

MAPPING FOR PMC AND XMC MODULES

VPX standardizes module expansion by formalizing carrier card pinouts for PMC and XMC daughter modules. A popular mezzanine format, PMC has been used extensively in Eurocard format designs in recent years.

VPX defines mappings for three of the most likely combinations:

- 3U/6U VPX carrier with PMC JN4 I/O mapping to backplane P2
- 3U/6U VPX carrier with XMC JN6 I/O mapping to backplane P2
- 6U VPX carrier with PMC JN4 I/O mapping to backplane P3 – P6

REAR TRANSITION MODULES

VPX anticipates the use of rear system I/O presented through the backplane instead of from the front of a module. Rear Transition Modules (RTMs) are a way to provide industry-standard connectors for on-board resources as a board designer confronts the

limited amount of space on the front panel. RTMs also permit an improved cabling configuration by allowing some or all cabling from a board to be routed out the rear of a chassis, providing unobstructed access to the faceplate. RTMs are defined in VPX under a dot specification.

Rear I/O is also preferred in most conduction- and liquid-cooled applications for serviceability and connector options.

VPX IN DEVELOPMENT AND USE

Mercury engineering teams are deeply involved in the definition of VPX, in several cases leading the development of key dot specifications. Many other organizations also support the efforts, including several leading embedded computing manufacturers and several major defense electronics system integration companies. This combination of architects from leading equipment vendors, integrators and users helped select best-of-breed concepts and technology from multiple existing and new standards developed for embedded computing products.

Along with Mercury Computer Systems, there are representatives from the following organizations participating in the working group efforts of the VPX standards development process. Many of these same companies have made product announcements in support of a robust ecosystem for VPX. These companies are also participating in the ongoing interoperability testing for VPX.

Aitech Defense Systems, Inc.

Amphenol Backplane Systems

The Boeing Company

Critia Computer, Inc.

Curtiss-Wright Controls Embedded Computing

Elma Bustronic Corporation

FCI Electronics

Foxconn Electronics Inc.

General Dynamics Advanced Information Systems

GE Fanuc

GHz Systems Inc.

Hybricon Corporation

IBSi

Motorola Embedded Communications Computing

Northrop Grumman Electronic Systems

Parker Hannifin

Pentair/Schroff

Radstone Embedded Computing

SBS Technologies, Inc.

Spectrum Signal Processing, Inc.

Tyco Electronics

U.S. Naval Surface Warfare Center, Crane Division (NSWC Crane)

CONCLUSION

VPX promises to be an exciting advancement for open architecture, embedded computing standards. It is based on years of experience gained from VMEbus technology advancements and field deployed systems. The specification has been carefully developed and validated by companies that have hundreds of years of combined experience in embedded computing.

VPX truly addresses the needs of high-performance embedded computing. The specification leaves plenty of room for evolutionary growth of VPX to ensure that it continues to be a viable solution for many years to come.

VPX also creates a path forward for today's VMEbus users, helping them evolve to next-generation technology while continuing to use the well-known, low-risk technology with which they're already familiar.

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